WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of multilevel memory cells, each cell storing at least three levels of data each;

arranging means for accepting at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and the second data being coded by a coding method, and for arranging the first and the second data bits in order that at least a bit of an N-order of the first data bits and a bit of the N-order of the second data bits are stored in one of the cells, the N being an integral number;

generating means for generating at least a voltage corresponding to the N-order bits; and

applying means for applying the voltage to the one of the cells in response to an address information corresponding to the one of the cells.

2. The semiconductor device according to claim 1, wherein the arranging means controls the number of the data bits to be stored in the one of the cells in accordance with error-correcting capability of the coding method.

3. The semiconductor device according to claim 1, wherein the arranging means puts an m number of the data bits having a length n in positions of m x n arrangement to store the m number of the data bits in each cell, m and n being an integral number.

4. The semiconductor device according to claim 1, wherein the multilevel memory cells are non-volatile semiconductor memories.

5. A method of writing data of bits in a semiconductor device having a plurality of multilevel memory cells, each cell storing at least three levels of data each, comprising

the steps of:

entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and the second data being coded by a coding method;

arranging the first and the second data bits such that at least a bit of an N-order of the first data bits and a bit of the N-order of the second data bits are stored in one of the cells, the N being an integral number;

generating at least a voltage corresponding to the N-order bits; and

applying the voltage to the one of the cells in response to an address information corresponding to the one of the cells.

6. A computer readable medium storing program code for causing a computer to write data of bits in a semiconductor device having a plurality of multilevel memory cells, each cell storing at least three levels of data each, comprising:

first program code means for entering at least a first data composed of a plurality of first data bits and a second data composed of a plurality of second data bits, the first and the second data being coded by a coding method; and

second program code means for arranging the first and the second data bits such that at least a bit of an N-order of the first data bits and a bit of the N-order of the second data bits are stored in one of the cells, the N being an integral number.

7. The computer readable medium according to claim 6 further comprising:

third program code means for generating at least a voltage corresponding to the N-order bits; and

fourth program code means for applying the voltage to the one of the cells in response to an address information

corresponding to the one of the cells.

8. A semiconductor device comprising:

converting means for converting a logical address into a physical address;

a plurality of multilevel memory cells arranged so as to correspond to a physical address space including the physical address, each cell storing 2^n levels of data each expressed by n ($n \geqq 2$) number of bits (X1, X2, ..., Xn);

judging means for judging whether a logical address space including the logical address matches the physical address space;

specifying means for specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when the logical address space matches the physical address space; and

outputting means for outputting the specified bit from one of the cells corresponding to the physical address.

9. The semiconductor device according to claim 8 wherein each cell includes at least one transistor and the specifying means comprises:

first means for generating a voltage corresponding to the reference value;

second means responsive to the physical address for generating an address signal;

third means responsive to the address signal for applying the voltage to one of the cells corresponding to the physical address;

fourth means for determining whether a current flows between a source and a drain of the transistor; and

fifth means for specifying the most significant bit X1 in accordance with a result of the determination.

10. The semiconductor device according to claim 8 wherein the specifying means comprises:

a comparator having a first input terminal connected

to an output of each cell, a voltage corresponding to the most significant bit X1 being applied to the first input terminal; and

a voltage applying circuit, connected to a second input terminal of the comparator, for applying the voltage corresponding to the reference value to the second input terminal, the most significant bit X1 being specified in accordance with a result of comparison by the comparator.

11. The semiconductor device according to claim 8 wherein the specifying means specifies the bits (X1, X2, ..., Xn), by n-time specifying operation maximum, by means of maximum n number of different reference values when judged that the logical address space does not match the physical address space.

12. The semiconductor device according to claim 11 wherein each cell includes at least one transistor and the specifying means comprises:

first means for generating n number of voltages corresponding to the n number of reference values;

second means responsive to the physical address for generating an address signal;

third means responsive to the physical address for applying the voltages to one of the cells corresponding to the address signal;

fourth means for applying maximum the n number of voltages to a gate of the transistor at a specific voltage applying order until a current flows between a source and a drain of the transistor; and

means for specifying the bits (X1, X2, ..., Xn) by detecting the current.

13. The semiconductor device according to claim 11 wherein the specifying means comprises:

a comparator having a first input terminal connected to an output of each cell, voltages corresponding to the

bits (X1, X2, ..., Xn) being applied to the first input terminal; and

a voltage applying circuit, connected to a second input terminal of the comparator, for applying voltages corresponding to maximum the n number of reference values to the second input terminal, the bits (X1, X2, ..., Xn) being specified in accordance with a result of comparison by the comparator.

14. A method of reading n ($n \geqq 2$) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising the steps of:

converting a logical address into a physical address included in the physical address space;

judging whether a logical address space including the logical address matches the physical address space;

specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space; and

outputting the specified bit from one of the cells corresponding to the physical address.

15. The method according to claim 14 further comprises the step of specifying the bits (X1, X2, ..., Xn), by n-time specifying operation maximum, by means of maximum n number of different reference values when judged that the logical address space does not match the physical address space.

16. A method of reading n ($n \geqq 2$) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ...,

and Xn), comprising the steps of:

converting a logical address into a physical address included in the physical address space;

judging whether a logical address space including the logical address matches the physical address space;

specifying the most significant bit X1 by applying a predetermined reference voltage to a gate of the transistor to determine whether a current flows between a source and a drain of the transistor when the logical address space matches the physical address space; and

outputting the specified bit from one of the cells corresponding to the physical address.

17. The method according to claim 16 further comprises the step of specifying the bits (X1, X2, ..., Xn) by applying maximum n number of different reference voltages to the gate of the transistor at a specific voltage applying order until a current flows between the source and the drain when judged that the logical address space does not match the physical address space.

18. A method of reading n ($n \geq 2$) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., and Xn), comprising the steps of:

converting a logical address into a physical address included in the physical address space;

judging whether a logical address space including the logical address matches the physical address space;

specifying the most significant bit X1 by comparing an output voltage of the transistor corresponding to the most significant bit with a reference voltage when the logical address space matches the physical address space; and

outputting the specified bit from one of the cells

corresponding to the physical address.

19. The method according to claim 18 further comprises the step of specifying the bits (X1, X2, ..., Xn) by comparing output voltages of the transistor corresponding to the bits (X1, X2, ..., Xn) with reference voltages corresponding to the bits (X2, ..., Xn).

20. A computer readable medium storing program code for causing a computer to read n ($n \geq 2$) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

first program code means for converting a logical address into a physical address included in the physical address space;

second program code means fop judging whether a logical address space including the logical address matches the physical address space;

third program code means for specifying the most significant bit X1, by one-time specifying operation, by means of a reference value when judged that the logical address space matches the physical address space; and

fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

21. The computer readable medium according to claim 20 further comprising program code means for specifying the bits (X1, X2, ..., Xn), by n-time specifying operation maximum, by means of maximum n number of different reference values when judged that the logical address space does not match the physical address space.

22. A computer readable medium storing program code for

causing a computer to read n (n ≧ 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

first program code means for converting a logical address into a physical address included in the physical address space;

second program code means for judging whether a logical address space including the logical address matches the physical address space;

third program code means for specifying the most significant bit X1 by applying a reference voltage to a gate of the transistor when the logical address space matches the physical address space to determine whether a current flows between a source and a drain of the transistor; and

fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

23. The computer readable medium according to claim 22 further comprising the program code means for specifying the bits (X1, X2, ..., Xn) by applying maximum n number of different reference voltages to the gate of the transistor at a specific voltage applying order until a current flows between the source and the drain when judged that the logical address space does not match the physical address space.

24. A computer readable medium storing program code for causing a computer to read n (n ≧ 2) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing

2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

first program code means for converting a logical address into a physical address included in the physical address space;

second program code means for judging whether a logical address space including the logical address matches the physical address space;

third program code means for specifying the most significant bit X1 by comparing an output voltage of the transistor corresponding to the most significant bit with a reference voltage when the logical address space matches the physical address space; and

fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

25. The computer readable medium according to claim 24 further comprising the program code means for specifying the bits (X1, X2, ..., Xn) by comparing voltages corresponding to the bits (X1, X2, ..., Xn) with reference voltages corresponding to the bits (X1, X2, ..., Xn) when judged that the logical address space does not match the physical address space.

26. A semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, the semiconductor device comprising a bit disperser for dispersing bits over the plurality of multilevel memory cells to store the bits therein, the bits constituting at least one code data coded by a coding method to be stored in the cells.

27. The semiconductor device according to claim 26, wherein the bit disperser controls the number of bits to be stored in at least one of the cells in accordance with

capability of code error correction of the coding method.

28. The semiconductor device according to claim 26, wherein the bit disperser puts the bits of M number of code data, each code data having a code length N, into positions of arrangement in M lines x N rows and stores the M number of bits in each cell, the M and N being an integral number.

29. The semiconductor device according to claim 26, wherein the multilevel memory cells are non-volatile semiconductor memories.

30. A computer readable medium storing program code for causing a computer to store data in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, comprising a program code means for dispersing bits over the plurality of multilevel memory cells to store the bits therein, the bits constituting at least one code data coded by a coding method to be stored in the cells.

31. A method of writing at least one code data coded by a coding method in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, the method comprising the step of dispersing bits constituting the code data over the plurality of multilevel memory cells.

32. A computer readable medium storing program code for causing a computer to write at least one code data coded by a coding method in a semiconductor device having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each, comprising the program code for dispersing bits constituting the code data over the plurality of multilevel memory cells.

33. A semiconductor device comprising:

inputting means for inputting a logical address;

converting means for converting the logical address into a physical address;

a plurality of multilevel memory cells arranged so as to correspond to physical addresses, each cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more;

controlling means for selecting one of the cells corresponding to the physical address and designating one of the data components in accordance with the logical address; and

outputting means for outputting the designated data component, wherein the semiconductor device has a judging value for specifying, by one-time specifying operation, at least one of the data components, and when the logical address is included in an address space A1 that corresponds to an address space including the physical address, the controlling means specifies the designated data component by means of the judging value, thus the specified data being output by the outputting means.

34. The semiconductor device according to claim 33, wherein each cell stores 2^n levels of data each expressed by data components (X1, X2, ..., Xn) of n - th dimension ($n \geqq 2$), the semiconductor device having a first judging value for specifying, by one-time specifying operation, at least the data component X1 having data of the logical address included in the address space A1, when the logical address included in the address space A1 is input by the inputting means, the data component X1 specified by the controlling means by means of the first judging value is output by the outputting means among the data components stored in the cell corresponding to the logical address included in the address space A1.

35. The semiconductor device according to claim 34, having

judging values for specifying the data components (X2, ..., Xn) of a logical address included in address spaces (A2, ..., An) close to the address space A1, wherein the data components (X2, ..., Xn) have the data stored sequentially in the order of closeness to the address space A1, the controlling means specifies a data component Xk (k = 1, 2,..., n), by k-time specifying operation, by means of the judging values in accordance with an address space including the logical address input by the inputting means, thus the data component Xk being output by the outputting means.

36. The semiconductor device according to claim 33, wherein each cell is provided with a control gate and a charge accumulating layer having a floating gate.

37. A method of reading data stored in a semiconductor device having at least one multilevel memory cell provided so as to correspond to a physical addresses converted from an input logical address, the cell having a control gate, a source and a drain, the cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more; comprising the steps of:

preparing a judging value for specifying at least one of the data components; and

applying a voltage corresponding to the judging value to the control gate to determine whether a current flows between the source and the drain when the logical address is included in an address space A1 that corresponds to an address space including the physical address.

38. The method according to claim 37, wherein the cell stores 2^n levels of data each expressed by data components (X1, X2, ..., Xn) of n - th dimension ($n \geqq 2$), the data component X1 having data of the logical address included in the address space A1, further comprising the steps of:

preparing a first judging value for specifying at least

the data component X1;

specifying the data component X1 by means of the first judging value among data components corresponding to the input logical address included in the address space A1; and

outputting the data component X1 specified by means of the first judging value among data components corresponding to the input logical address included in the address space A1.

39. The method according to claim 38, further comprising the steps of:

preparing judging values for specifying the data components (X2, ..., Xn) having data of logical addresses included in address spaces (A2, ..., An) close to the address space A1, the data components (X2, ..., Xn) having the data stored sequentially in the order of closeness to the address space A1;

specifying a data component Xk (k = 1, 2,..., n), by k-time specifying operation, by means of the judging values in accordance with an address space including an input logical address; and

outputting the data component Xk.

40. A computer readable medium storing program code for causing a computer to read data stored in a semiconductor device having at least one multilevel memory cell provided so as to correspond to a physical addresses converted from an input logical address, the cell having a control gate, a source and a drain, the cell storing at least three levels of data each, the data being expressed by data components of two-dimension or more; comprising:

first program code means for preparing a judging value for specifying at least one of the data components; and

second program code means for applying a voltage corresponding to the judging value to the control gate to determine whether a current flows between the source and the drain when the logical address is included in an

address space A1 that corresponds to an address space including the physical address.

41. The computer readable medium according to claim 40, wherein the cell stores 2^n levels of data each expressed by data components (X1, X2, ..., Xn) of n - th dimension (n $\geqq$ 2), the data component X1 having data of the logical address included in the address space A1, further comprising:

third program code means for preparing a first judging value for specifying at least the data component X1;

fourth program code means for specifying the data component X1 by means of the first judging value among data components corresponding to the input logical address included in the address space A1; and

fifth program code means for outputting the data component X1 specified by means of the first judging value among data components corresponding to the input logical address included in the address space A1.

42. The computer readable medium according to claim 41, further comprising:

sixth program code means for preparing judging values for specifying the data components (X2, ..., Xn) having data of logical addresses included in address spaces (A2, ..., An) close to the address space A1, the data components (X2, ..., Xn) having the data stored sequentially in the order of closeness to the address space A1;

seventh program code means for specifying a data component Xk (k = 1, 2,..., n), by k-time specifying operation, by means of the judging values in accordance with an address space including an input logical address; and

eighth program code means for outputting the data component Xk.

43. A semiconductor device comprising:

a plurality of multilevel memory cells, each cell

storing one of at least three different levels of data each;

first coding means for converting, by a coding method, a first data into a first code composed of at least two-digit code components;

second coding means for converting, by a coding method, a second data into a second code composed of at least two-digit code components; and

arranging means for arranging the code components in order to store at least two pairs of code components in corresponding cells, each pair having a code component of the first code and a code component of the second code of a same digit.

44. The semiconductor device according to claim 43 wherein the first and the second codes are of the same number of digits.

45. The semiconductor device according to claim 43 wherein the coding method employs the binary system.

46. The semiconductor device according to claim 43 wherein each cell includes a control gate and a floating gate.

47. The semiconductor device according to claim 43 wherein the cells are at least a member of the group consisting of an MNOS, a mask ROM, an EEPROM, an EPROM, a PROM, and a non-volatile flash memory.

48. The semiconductor device according to claim 43 further comprising correction means for correcting at least an error occurring in the first code.

49. A semiconductor device comprising:

a plurality of multilevel memory cells, each cell storing one of at least three different levels of data

each;

coding means for converting input data into a code of at least two digits by a coding method; and

separating means for separating the code by a specific number of digits into at least a first and a second block of code components to store at least a code component group in at least one of the cells, the group having a code component of the first block and a code component of the second block of a same digit.

50. The semiconductor device according to claim 49 further comprising reading means for reading the code components stored in the cells and correcting at least one code train composed of the code components under error correction capability of the coding method to output the corrected code train.

51. The semiconductor device according to claim 50, wherein the reading means reads a data bit of a specific digit from each cell to form the code train.

52. The semiconductor device according to claim 51, wherein each cell storing one of four different levels of data each and the separating means separates the code into a first and a second block of code components of a same number of digit to store a code component pair at least in one of the cells, the pair having a code component of the first block and a code component of the second block of a same digit.

53. The semiconductor device according to claim 52, wherein each of the two blocks is composed of data bits with redundant bits when the blocks are output.

54. The semiconductor device according to claim 53, wherein the redundant bits are formed on the basis of the two blocks so as to correspond to each of the two blocks,

the total number of the number of the data bits of each of the two blocks and the number of the corresponding redundant bits being equal to the number of bits of the code train.

55. The semiconductor device according to claim 51, wherein each cell stores one of eight different levels of data each and the separating means separates the code into a first, a second and a third block of code components of a same number of digit to store a code component group in at least one of the cells, the group having a code component of the first block, a code component of the second block and a code component of the third block of a same digit.

56. The semiconductor device according to claim 55, wherein each of the three blocks is composed of data bits with redundant bits when the blocks are output.

57. The semiconductor device according to claim 56, wherein the redundant bits are formed on the basis of the three blocks so as to correspond to each of the three blocks, the total number of the number of the data bits of each of the three blocks and the number of the corresponding redundant bits being equal to the number of bits of the code train.

58. The semiconductor device according to claim 56, wherein the redundant bits include first redundant bits formed on the basis of second redundant bits formed by means of Hamming code so as to correspond to each of the three blocks, the second redundant bits being added to each of the three blocks to form code trains, all bits of each code train being EX-ORed to form the first redundant bits so as to correspond to each code train, the total number of the number of the bits of each code train and the number of the corresponding first redundant bits being equal to

the number of bits of the code train.

59. The semiconductor device according to claim 55, wherein the first block is composed of data bits with redundant bits and a fourth block formed by connecting the second and the third blocks is composed of data bits with redundant bits when the first and the fourth blocks are output.

60. The semiconductor device according to claim 59, wherein the redundant bits are formed on the basis of the first, the second and the third blocks so as to correspond to the first and the fourth blocks, the total number of the number of the data bits of the first block and the number of the corresponding redundant bits and the total number of the number of data bits of two blocks formed by dividing the fourth block and the number of the corresponding redundant bits being equal to the number of bits of the code train.

61. The semiconductor device according to claim 51, wherein each cell storing one of sixteen different levels of data each and the separating means separates the code into a first, a second, a third and a fourth block of code components of a same number of digit to store a code component group in at least one of the cells, the group having a code component of the first block, a code component of the second block, a code component of the third block and a code component of the fourth block of a same digit.

62. The semiconductor device according to claim 61, wherein each of the four blocks is composed of data bits with redundant bits when the blocks are output.

63. The semiconductor device according to claim 62, wherein the redundant bits are formed on the basis of the four blocks so as to correspond to each of the four blocks,

the total number of the number of the data bits of each of the four blocks and the number of the corresponding redundant bits being equal to the number of bits of the code train.

64. The semiconductor device according to claim 63, wherein the redundant bits include first redundant bits formed on the basis of second redundant bits formed by means of Hamming code so as to correspond to each of the four blocks, the second redundant bits being added to each of the four blocks to form code trains, all bits of each code train being EX-ORed to form the first redundant bits so as to correspond to each code train, the total number of the number of the bits of each code train and the number of the corresponding first redundant bits being equal to the number of bits of the code train.

65. The semiconductor device according to claim 61, wherein a fifth block formed by connecting the first and the second blocks and a sixth block formed by connecting the third and the fourth blocks are composed of data bits with redundant bits when the fifth and the sixth blocks are output.

66. The semiconductor device according to claim 65, wherein the redundant bits are formed on the basis of the first, the second, the third and the fourth blocks so as to correspond to the fifth and the sixth blocks, the total number of the number of the data bits of each of two blocks formed by dividing each of the fifth and the sixth blocks and the number of the corresponding redundant bits being equal to the number of bits of the code train.

67. The semiconductor device according to claim 49 wherein each cell includes a control gate and a floating gate.

68. The semiconductor device according to claim 49 wherein

the cells are at least a member of the group consisting of an MNOS, a mask ROM, an EEPROM, an EPROM, a PROM, and a non-volatile flash memory.